



PATENT
Attorney Docket No. ASC-044C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Fitzgerald *et al*
SERIAL NO.: 10/611,739 GROUP NO.: 2818
FILING DATE: July 1, 2003 EXAMINER: Le, Dung Anh
TITLE: METHOD OF FABRICATING CMOS INVERTER AND
INTEGRATED CIRCUITS UTILIZING STRAINED SILICON
SURFACE CHANNEL MOSFETS

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

The references listed on the enclosed PTO-1449 and enclosed herewith are submitted solely in compliance with the duty of candor. It is understood that this Information Disclosure Statement does not fall within the provisions of 37 C.F.R. §1.97. Please note that reference A157 has previously been cited to the U.S. Patent and Trademark Office by its U.S. patent application serial number in an Information Disclosure Statement filed for the above-referenced application. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98(a)(2)(i), only copies of the foreign patent documents and non-patent publications are enclosed.

In addition, Applicants wish to inform the Examiner about the following co-pending patent applications and Office Actions cited therein:

- 1) U.S. Serial No. 09/611,024 (Docket No. ASC-023C1) filed on 06/07/2000, by Fitzgerald;
- 2) U.S. Serial No. 10/774,890 (Docket No. ASC-049C1) filed on 02/09/2004, by Fitzgerald;
- 3) U.S. Serial No. 10/802,185 (Docket No. ASC-025DVC1) filed on 03/17/2004, by Cheng *et al.*;
- 4) U.S. Serial No. 10/802,186 (Docket No. ASC-025DV2C1) filed on 03/17/2004, by Cheng *et al.*;
- 5) U.S. Serial No. 10/826,156 (Docket No. ASC-023C2) filed on 04/16/2004, by Fitzgerald; and
- 6) U.S. Serial No. 10/854,556 (Docket No. ASC-054C1) filed on 05/26/2004, by Fitzgerald.

Supplemental Information Disclosure Statement

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It is respectfully requested that the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

Respectfully submitted,

Date: August 17, 2007

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